

General Description

The A8012 is a 12-channel, constant current sink, LED driver. An external resistor set the maximum current value of all channels. 40V Vout allow people to serial link 12pcs of LED in one channel. 40MHz clock frequency allows people to run in higher clock rate. A thermal protection function is featured to prevent over-heating.

Key Features

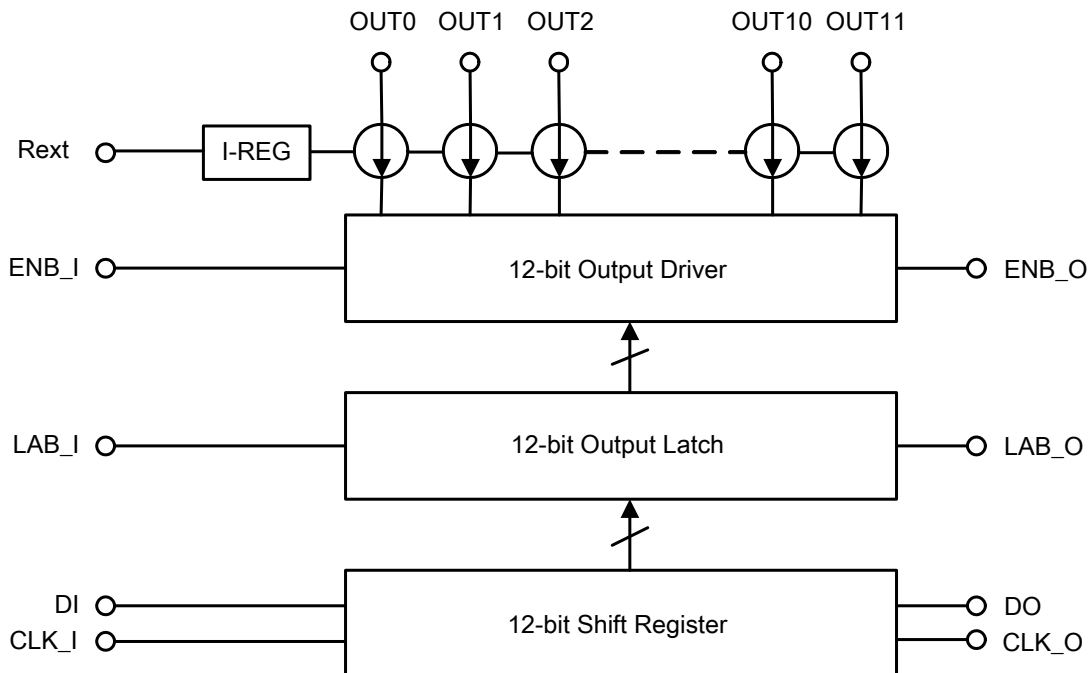
- 12 Constant Current Output Channels
- Driver Capability – 0 to 40mA (Current Sink)
- 3V/5V SPI interface for serial input and output
- 40MHz clock frequency
- Fast response of output current, pulse width(min): 200ns
- Power supply voltage range $V_{DD} = 5.0V$ to 24V

- Current Accuracy:
 - $\pm 3\%$ (Channel to Channel)
 - $\pm 6\%$ (Chip to Chip)
- DATA, LATCH, CLK, output enable using cascade interface
- $V_{out} = 40V$
- Operating Temperature: $-40^{\circ}C$ to $85^{\circ}C$
- Integrated Over-Temperature Protection
- Package : SSOP 24, PDIP 24

Applications

- Side Light controller
- Direct Back Lighting controller
- Main Lighting
- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards

Block Diagram





Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	27	V
Input Voltage	V_{IN}	7	V
Output Current	I_O	45	mA/channel
Output Voltage	V_{OUT}	-0.4 ~ 45.0	V
Power Dissipation	P_D	1.42	W
Thermal Resistance	$R_{TH(i-a)}$	70.45	°C/W
ESD(HBM)	-	2K	V
Operating Temperature	T_A	-40 ~ 85	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	4.5	-	24.0	V
Output Voltage	V_{OUT}	OUT ₀ ~ OUT ₁₁	1.0	-	40.0	V
Output Current	I_{OUT}	Each DC circuit	0	-	40	mA/ch
Clock frequency	f_{CLK}	Cascade connected	-	-	40M	Hz
LAB_I pulse width	$t_{W(L)}$		25	-	-	ns
CLK_I pulse width	$t_{W(CLK)}$	-	12.5	-	-	ns
ENB_I pulse width	$t_{W(E)}$	$I_{OUT} = 20mA$	200	-	-	ns

Electrical Characteristics

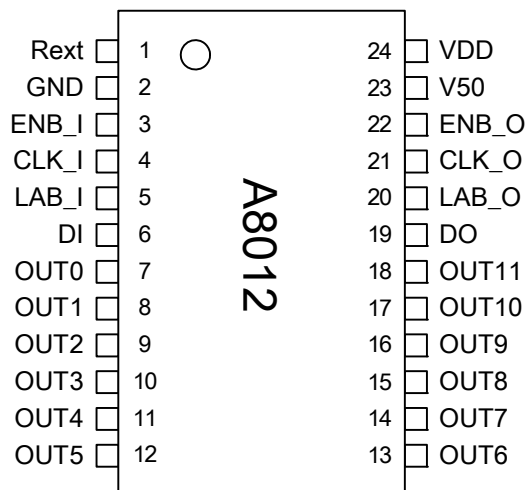
Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	4.5	-	24.0	V
Output Voltage	V_{OUT}	OUT ₀ ~ OUT ₁₁	-	-	40.0	V
Supply Current	I_{DD}	No data transfer, All outputs OFF $R_{EXT} = 890\Omega$	-	-	8	mA
Input Voltage	V_{IH}	-	2.0	-	5.5	V
	V_{IL}	-	GND	-	0.8	V
Output Voltage	V_{OH}	$I_{OH} = -8mA$	2.4	-	-	V
	V_{OL}	$I_{OL} = 8mA$	-	-	0.4	V
Output Leakage Current	I_{OL}	$V_{OH}=40V, OUT_0 \sim OUT_{11}$	-	-	1	μA
Constant Output Current	I_{OUT1}	$V_{OUT}=1.0V$ $V_{DD}=5 \sim 24V$ $R_{EXT} = 890\Omega$	-	20.0	-	mA
Current Skew	ΔI_O	-	-	-	±3	%
Load Regulation	$\Delta I_{O(2)}$	-	-	±2	±6	%/V
Power Supply Rejection Ratio, PSRR	$\Delta I_{O(3)}$	-	-	±2	±6	%/V
Thermal protect threshold	T_j	Junction temperature	-	-	150	°C
Internal Pull-Low Resistor	R_{IN-L}	ENB_I, CLK_I, LAB_I, DI	-	150k	-	Ω



AC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock high pulse width	$t_{w(CLK)}$	-	12.5	-	-	ns
Data input setup time	$t_{SU(D)}$	DI – CLK_I	5	-	-	ns
Data input hold time	$t_{H(D)}$	CLK_I – DI	5	-	-	ns
LAB_I pulse width time	$t_{w(L)}$	-	25	-	-	ns
LAB_I setup time	$t_{SU(L)}$	CLK_I – LAB_I	25	-	-	ns
ENB_I pulse width	$t_{w(E)}$	-	200	-	-	ns
DO delay time	t_{pLH} , t_{pHL}	CLK_I – DO ($C_{Load} = 100pF$)	-	-	10	ns
OUTn delay time	t_{pLH2} , t_{pHL2}	ENB_I – OUTn	-	-	50	ns
Logic signal input to output delay time	t_{dLH} , t_{dHL}	CLK_I – CLK_O LAB_I – LAB_O ENB_I – ENB_O ($C_{Load} = 100pF$)	-	-	10	ns

Pin Configuration



Terminal Description

Pin number	Pin name	I/O	Description
1	Rext	I	Connect an external resistor to setup output current.
2	GND	G	Ground
3	ENB_I	I	Output enable. When ENB_I is driven Low, all outputs are enabled. When ENB_I is driven High, all outputs are turned OFF.
4	CLK_I	I	Clock input for data shift on rising edge.
5	LAB_I	I	Data latch. When LAB_I is driven High, the data in shift register is transferred to the output latch. When LAB_I is driven Low, the data is latched in the output latch.

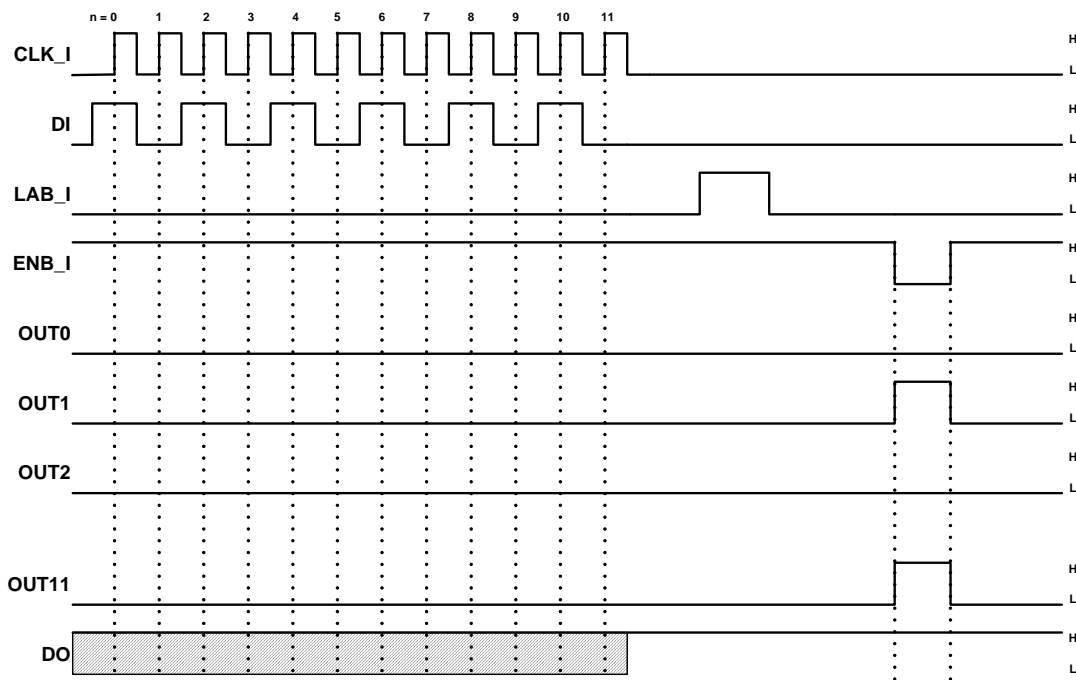


6	DI	I	Serial data input
7	OUT0	O	Constant current output 0
8	OUT1	O	Constant current output 1
9	OUT2	O	Constant current output 2
10	OUT3	O	Constant current output 3
11	OUT4	O	Constant current output 4
12	OUT5	O	Constant current output 5
13	OUT6	O	Constant current output 6
14	OUT7	O	Constant current output 7
15	OUT8	O	Constant current output 8
16	OUT9	O	Constant current output 9
17	OUT10	O	Constant current output 10
18	OUT11	O	Constant current output 11
19	DO	O	Serial data output to next driver
20	LAB_O	O	Output of data latch to next driver
21	CLK_O	O	Output of clock to next driver
22	ENB_O	O	Output of output enable to next driver
23	V50	O	Internal 5V regulator output. Connect a 1 μ F capacitor to GND.
24	VDD	P	Power supply

Truth Table

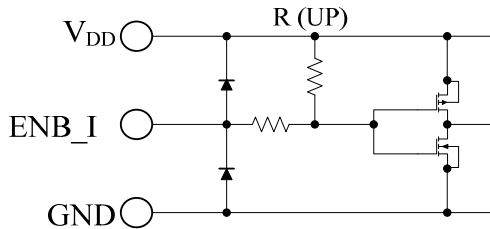
CLK_I	LAB_I	ENB_I	SERIAL-IN	OUT0 .. OUT5 ... OUT11	SERIAL-OUT
	H	L	Dn	Dn ... Dn-5 ... Dn-11	Dn-12
	L	L	Dn+1	No Change	Dn-11
	H	L	Dn+2	Dn+2 ... Dn-3 ... Dn-9	Dn-10
	X	L	Dn+3	Dn+2 ... Dn-3 ... Dn-9	Dn-9
	X	H	Dn+3	OFF	Dn-9

Timing Diagram

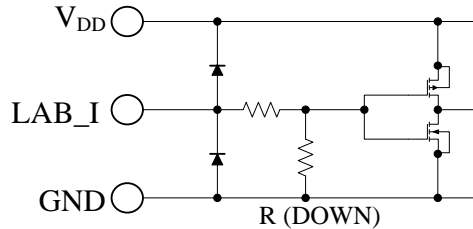


Equivalent Circuits for Inputs and Outputs

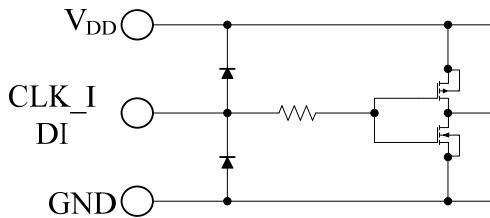
1. ENABLE terminal



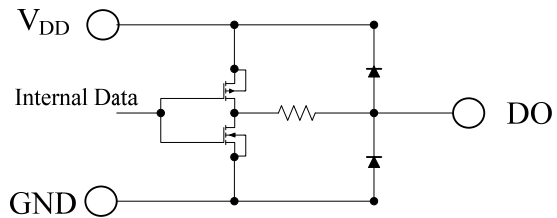
2. LATCH terminal



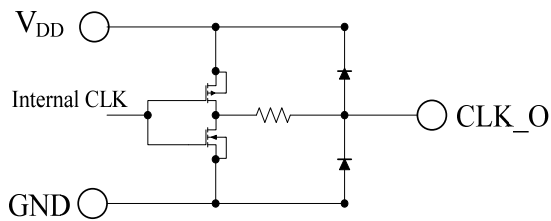
3. CLOCK, SERIAL-IN terminal



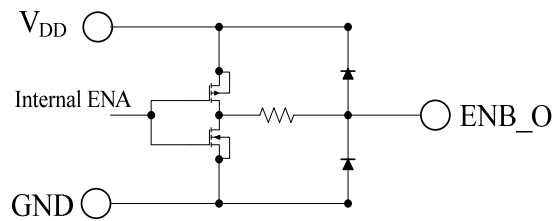
4. SERIAL-OUT terminal



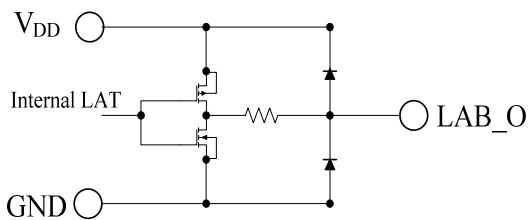
5. CLOCK-OUT terminal



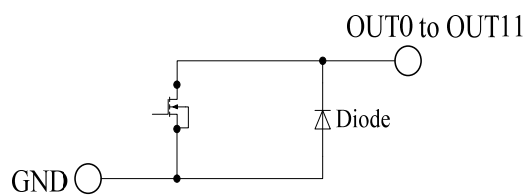
6. ENABLE-OUT terminal



7. LATCH-OUT terminal

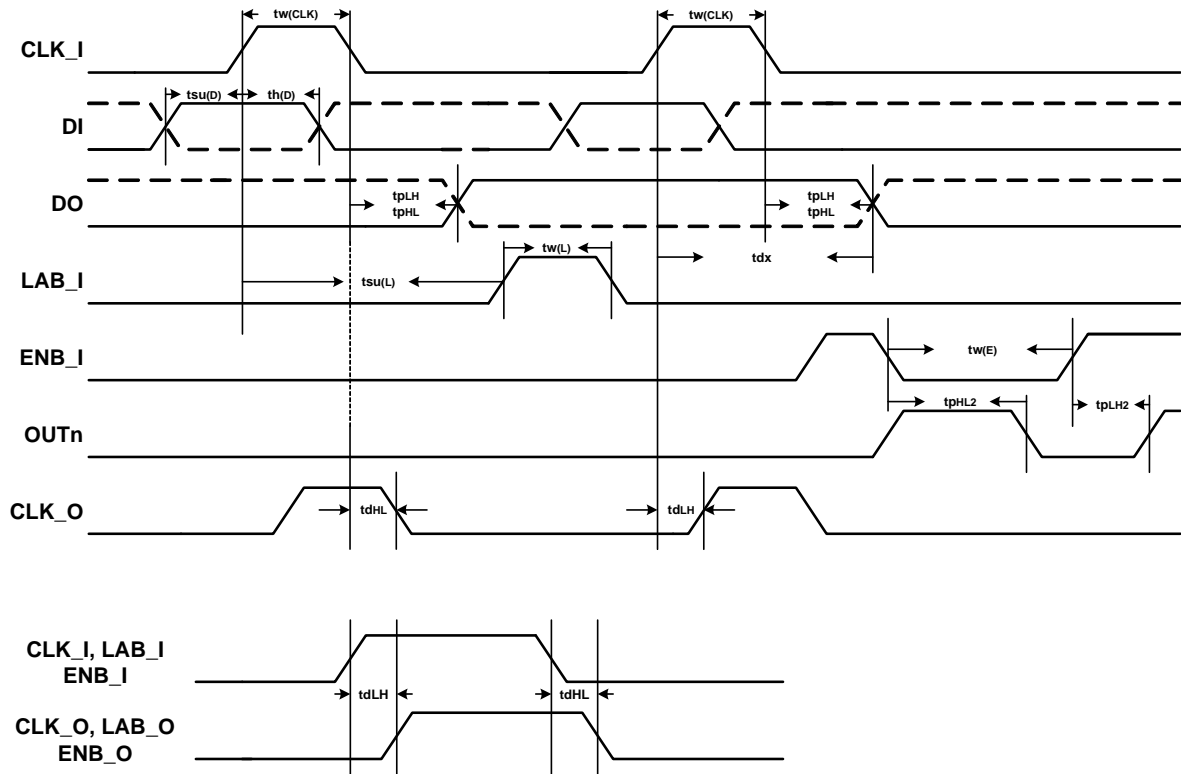


8. OUT0 to OUT11 terminal

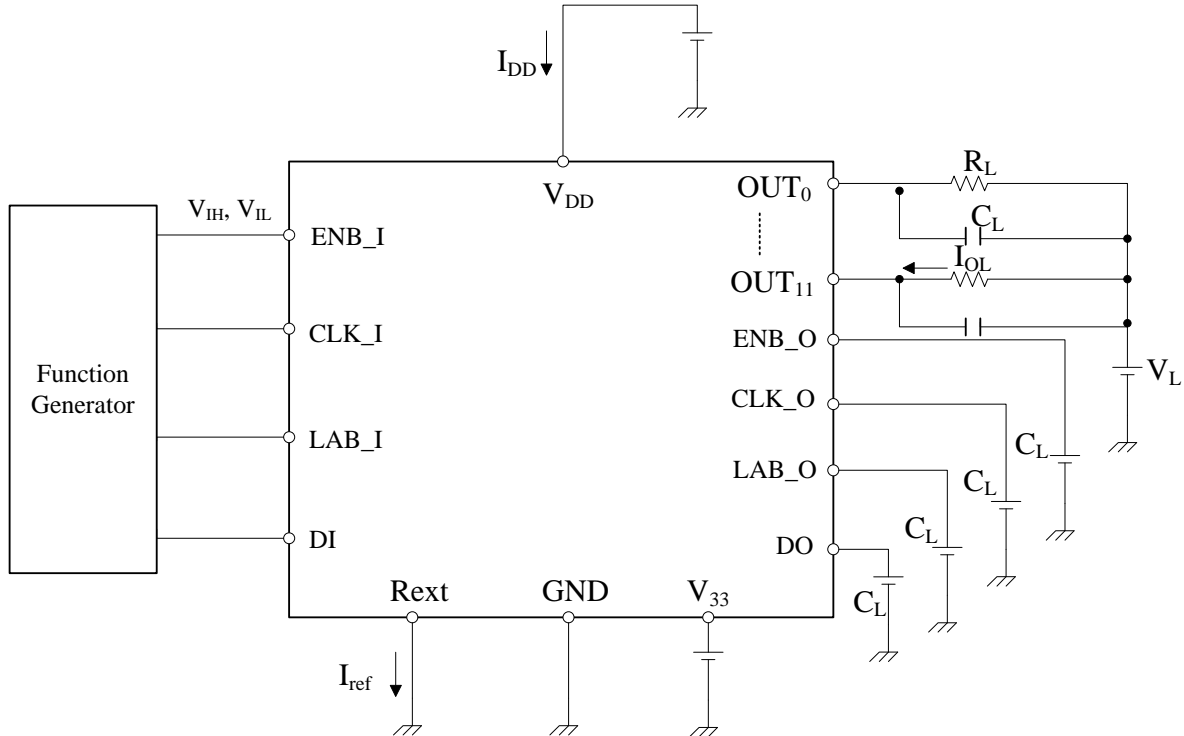




Timing Waveforms

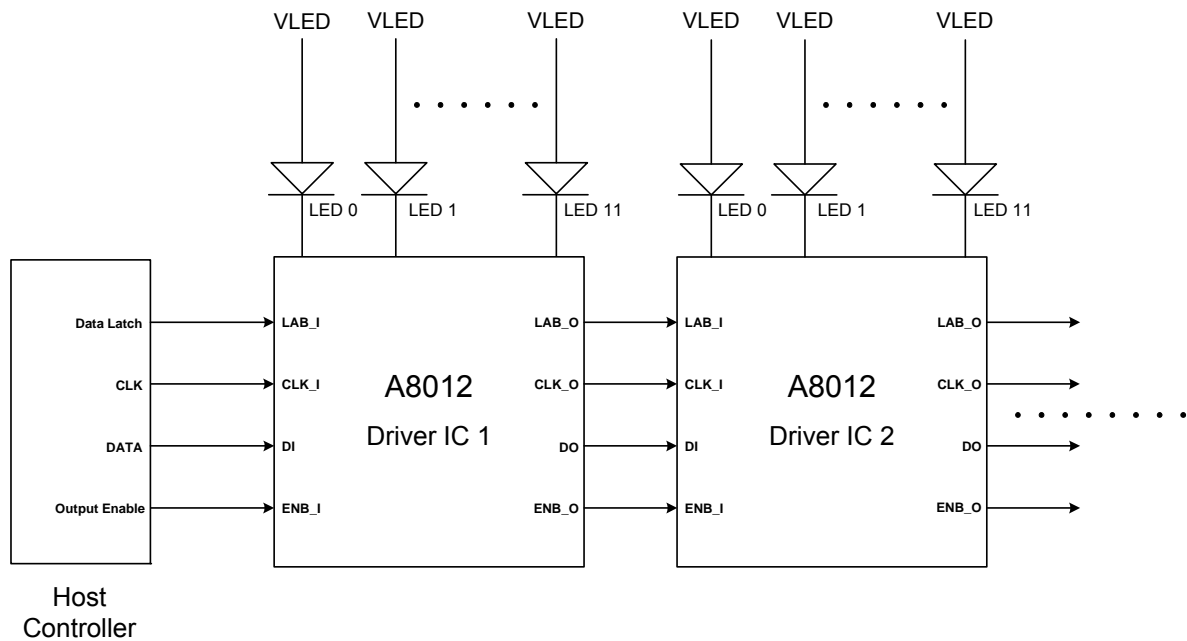


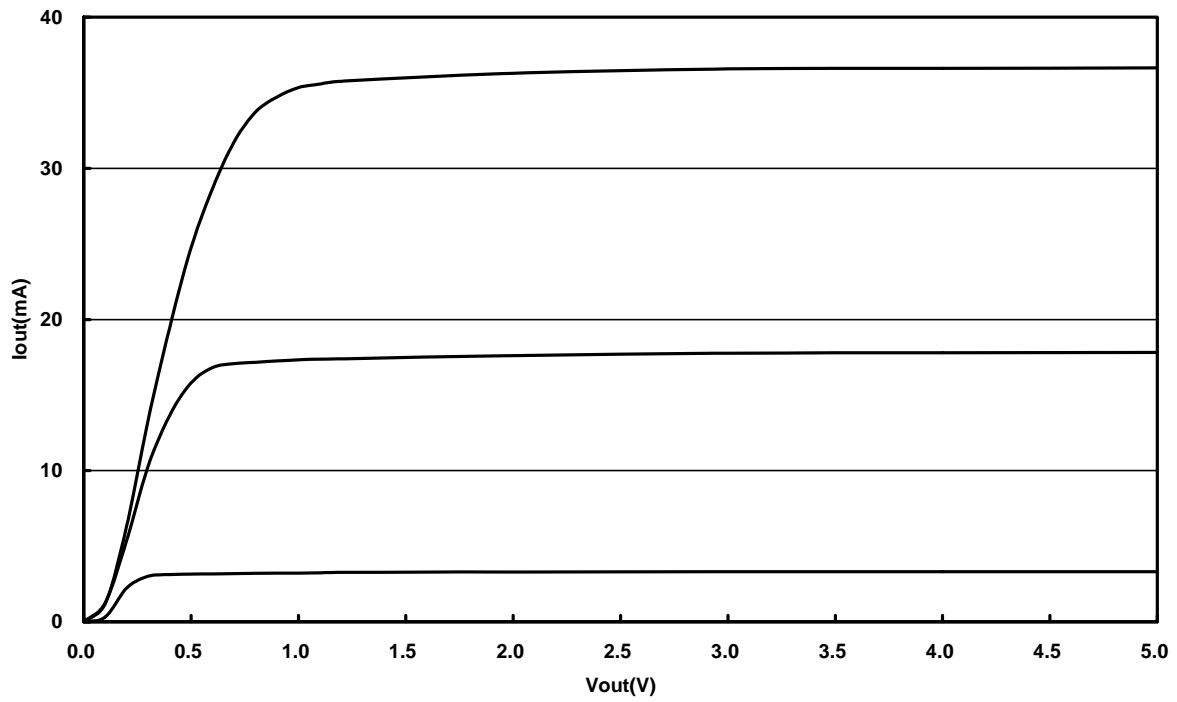
Test Circuit



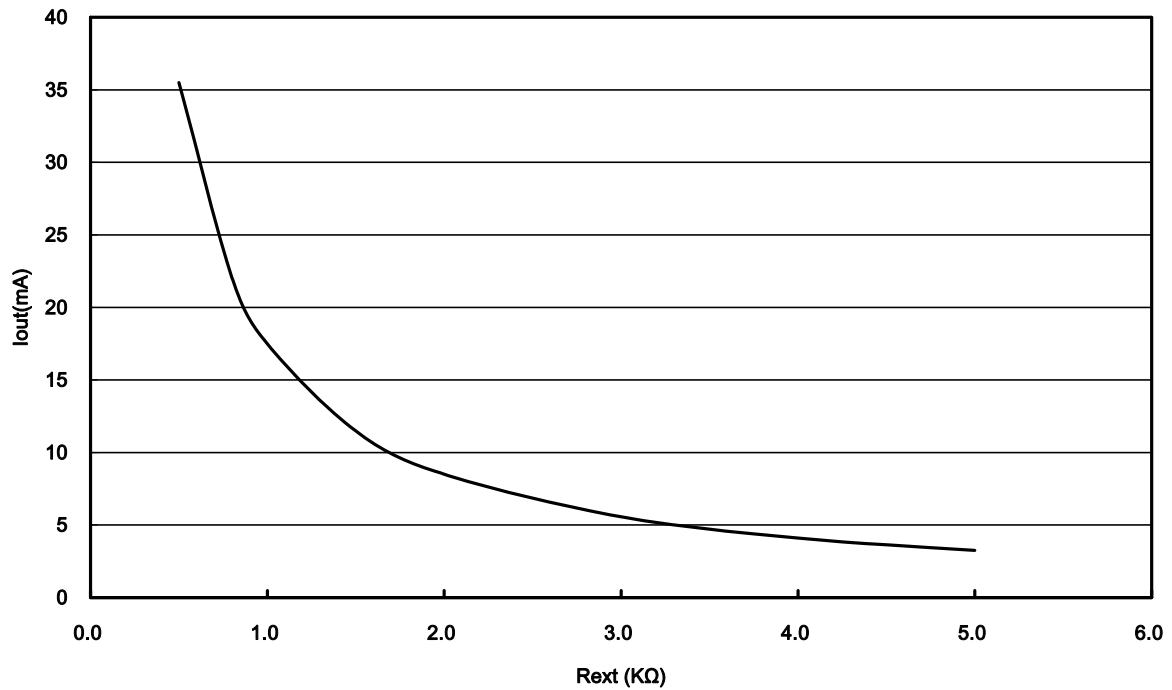
$V_{DD} = 5.0V$, $V_{IH} = 5.0V$, $V_{IL} = 0V$, $t_r = t_f = 10ns$, $C_L = 100pF$

Application Diagram



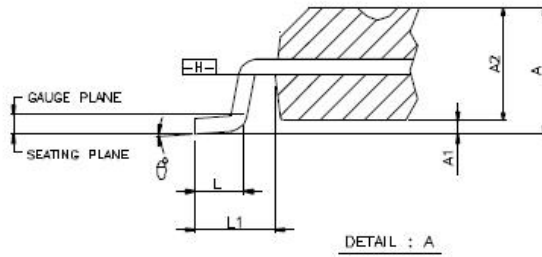
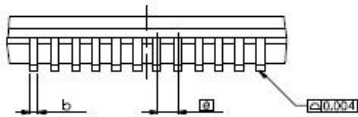
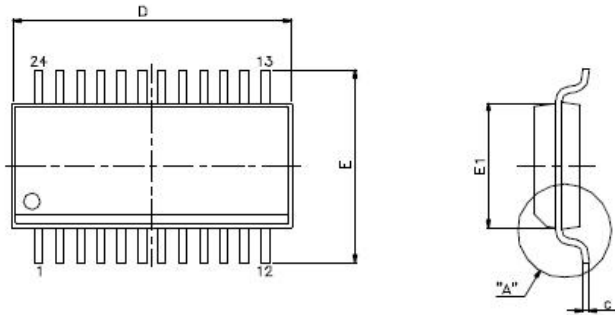


Output Current vs Output Voltage



I_{out} vs R_{ext} (I_{out} = 1.23 * 14.5 / R_{ext})

Package Dimension: SSOP24



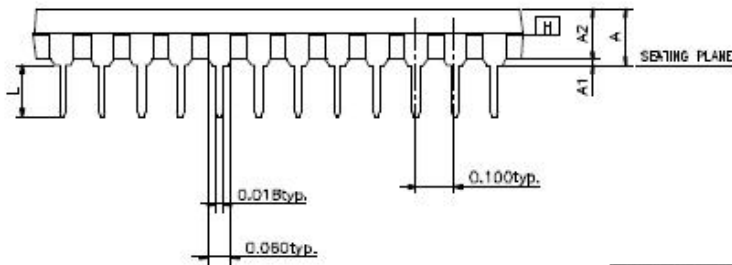
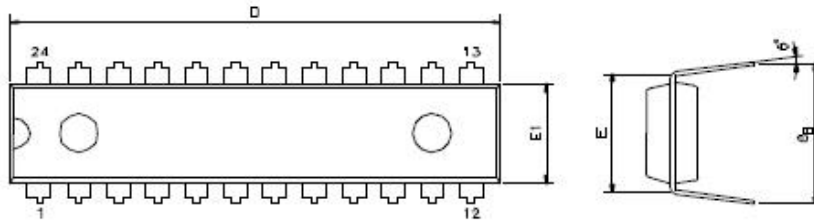
SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	—	—	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	—	0.012
C	0.007	—	0.010
⌀	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	—	8°

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MO-137 AE
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.

PDIP24



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E	0.300 BSC.		
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e _B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH